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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,935	04/01/2004	Todd P. Oman	DP-311231	2934

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EXAMINER
CARPIO, IVAN HERNAN

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,935	OMAN ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1-5 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (US patent 5936843).

With respect to claim 1, Ohshima teaches a ceramic substrate (Fig. 3, element 30) with a first surface (Fig. 3, the left vertical surface) and a lateral surface (Fig. 3, element 30 the walls surrounding the 1st surface) surrounding the first surface, an organic substrate (Fig. 3, element 32) with a first surface (Fig. 3, the entire outside surface, including the bottom and left side) and a lateral surface (Fig. 3, element 32 the walls surrounding the 1st surface) surrounding the first surface. A portion of the lateral surface of the organic substrate being adjacent to a portion of the lateral surface of the ceramic substrate (Fig. 3, note the bottom surface of the ceramic substrate and the top surface of the organic substrate are adjacent) so as to define an interface there between. At least one conductor (Fig. 3, element 32a-1) common to both the ceramic and organic substrates so as to physically connect the organic and ceramic substrates together, the conductor bridging the interface between the ceramic and organic substrates. Ohshima does not teach that at least one circuit component is on the first

surface of the ceramic substrate. It is well known to put circuit components on ceramic boards as taught by Ohshima (column 1, lines 23-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to place a circuit component on the first surface of the ceramic board for the purpose of maximizing the useful surface area of the ceramic board.

With respect to claim 2 and with all the limitations of claim 1, Ohshima teaches that the organic substrate comprises multiple dielectric layers (Fig. 3, elements 32b-1-5) and the conductor is buried with in the dielectric layers of the organic substrate.

With respect to claim 3 and with all the limitation of claim 1, Ohshima teaches all of the limitations except that the conductor is on the first surface of the ceramic substrate and is electrically connected to the circuit component on the ceramic substrate. One can extend the conductor 32a-1 in anyway necessary for making the proper electrical connections including extending it to the first surface of the ceramic substrate to electrically connect the circuit component. It would have been obvious to one of ordinary skill in the art at the time of the invention to extend the conductor to the first surface of the ceramic surface for the purpose of electrically connecting the circuit component on the ceramic surface to other circuit elements.

With respect to claim 4 and with all the limitations of claim 1, Ohshima teaches that the ceramic substrate has a coefficient of thermal conductivity that is greater than the coefficient of thermal conductivity of the organic substrate. Note that Ohshima teaches that the ceramic board can be Mullite (column 4, lines 67) and the organic board can be Teflon (column 4, line 7), which satisfies the criteria.

With respect to claim 5 and with all the limitations of claim 1, Ohshima teaches that the conductor patterns (Fig. 3, elements 32a-2-5) of the organic substrate is denser the conductor patterns (Fig. 3, elements 32a-1) of the ceramic substrate.

With respect to claim 11 and with all the limitations of claim 1, Ohshima teaches that the organic substrate comprises a second conductor (Fig. 3, element 34-1) and the common conductor overlays and is soldered (Fig. 3, element 38) to the second conductor.

With respect to claim 12 and 13 and with all the limitations of claim 1, Ohshima teaches all of the limitations including that the organic substrate comprises a through-hole (Fig. 3, element 36) and that it connects to the common conductor solderlessly. Ohshima does not teach that the through-hole is a plated through-hole. Plated through-holes are well known in the art and are used in many applications as connecting vias. It would have been obvious to one of ordinary skill in the art at the time of the invention to us plated through-holes for the purpose of making the electrical connection to the common conductor. For claim 13 Ohshima does not teach that the through-hole is soldered to the common conductor. Soldering is well known in the art and is used in many circuit board applications to electrically bond and connect separate elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to solder the through-hole to the common conductor because then one could make the through-hole and common conductor as separate parts and solder them together during manufacture to electrically connect the two.

With respect to claim 14 and with all the limitations of claim 1, Ohshima teaches that the ceramic and organic substrates are substantially coplanar and the portion of the lateral surface of the ceramic substrate abuts and contacts the portion of the lateral surface of the organic substrate. Fig. 3.

Claims 6-10 and15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima in view of Koors (US Patent 6365964).

With respect to claim 6 and with all the limitations of claim 1, Ohshima teaches all of the limitations except that a heatsink is in thermal contact with a surface of the circuit component oppositely disposed from the ceramic device. Koors teaches a heatsink (Figure, element 26) in thermal contact with a component (Figure, element 12) oppositely disposed from a substrate (Figure, element 16). It would have been obvious to one of ordinary skill in the art at the time of the invention to place the heat sink, taught by Koors, in thermal contact with the circuit component of the ceramic substrate taught by Ohshima for the purpose of cooling the component.

With respect to claim 7 and with all the limitations of claim 1, Ohshima teaches all of the limitations including that a circuit component (Fig. 3, element 14) is on the organic substrate. Ohshima does not teach that the circuit component is disposed on the first surface of the organic substrate and that a heatsink is in thermal contact with a surface of the circuit component oppositely disposed from the organic substrate. One can place a circuit component anywhere desired on a substrate including the "first surface" of a

substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the circuit component taught by Ohshima on the first surface of the organic substrate for the purpose of maximizing the useful surface area of the substrate. Furthermore Koors teaches a heatsink in thermal contact with a component oppositely disposed from a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the heat sink, taught by Koors, in thermal contact with the circuit component of the organic substrate taught by Ohshima for the purpose of cooling the component.

With respect to claim 8 and 9 and with all the limitations of claim 1, Ohshima teaches all of the limitations except that the ceramic and organic substrates are housed within a casing comprising first and second casing members, the first casing member supporting the ceramic substrate and the second casing member having a first heatsink pedestal and a second heat sink pedestal in thermal contact with a surface of the circuit component oppositely disposed from the ceramic substrate and organic substrate reseptively. Koors teaches a substrate (Figure, element 16) with components (Figure, elements 12) a casing comprising a 1st casing (Figure, element 22) and a 2nd casing (Figure, element 20), a 1st casing supporting the substrate (figure, element 30) and the 2nd casing having heatsink pedestals (figure, elements 26 left and right side) in thermal contact with components. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the substrates taught by Ohshima in the casing taught by Koors for the purpose of protecting the substrate while removing excessive heat from the components on the substrates.

With respect to claim 10 and with all the limitations of claim 9, Koors teaches that the 1st case has a pedestal (Figure, element 30) in thermal contact with a substrate oppositely disposed from a component. It would have been obvious to one of ordinary skill in the art to place the organic substrate on the pedestal for the purpose of allowing air to surround the substrate and allowing heat escape.

With respect to claim 15, Ohshima teaches a ceramic substrate (Fig. 3, element 30) with a first surface (Fig. 3, the left vertical surface) and a lateral surface (Fig. 3, element 30 the walls surrounding the 1st surface) surrounding the first surface, an organic substrate (Fig. 3, element 32) with a first surface (Fig. 3, the entire outside surface, including the bottom and left side) and a lateral surface (Fig. 3, element 32 the walls surrounding the 1st surface) surrounding the first surface. A portion of the lateral surface of the organic substrate being adjacent to a portion of the lateral surface of the ceramic substrate (Fig. 3, note the bottom surface of the ceramic substrate and the top surface of the organic substrate are adjacent) so as to define an interface there between. At least one conductor (Fig. 3, element 32a-1) common to both the ceramic and organic substrates so as to physically connect the organic and ceramic substrates together, the conductor bridging the interface between the ceramic and organic substrates. And a circuit component (Fig. 3, element 14) on the organic substrate. And that the ceramic substrate has a coefficient of thermal conductivity that is greater than the coefficient of thermal conductivity of the organic substrate. Note that Ohshima teaches that the ceramic board can be Mullite (column 4, lines 67) and the organic board can be Teflon (column 4, line 7), which satisfies the criteria. Oshima does not

teach that the ceramic substrate has a power integrated chip that dissipates more than 5 watts on the first surface, or that the organic substrate has at least one circuit component on a first surface thereof, or a casing comprising first and second casing members, a first heatsink pedestal defined by the second casing member and in thermal contact with a surface of the power integrated circuit chip on the ceramic substrate, and a second heatsink pedestal defined by the second casing member and in thermal contact with a surface of the circuit component on the organic substrate. It is well known to put circuit components, including power integrated circuit that dissipate at least 5 watts on ceramic boards as taught by Ohshima (column 1, lines 23-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to place a power integrated circuit component on the first surface of the ceramic board for the purpose of accomplishing a desired circuit arrangement and maximizing the useful surface area of the ceramic board. With respect to the circuit component on the organic substrate one can place a circuit component anywhere desired on a substrate including the "first surface" of a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the circuit component taught by Ohshima on the first surface of the organic substrate for the purpose of maximizing the useful surface area of the substrate. With respect to the casing, Koors teaches a substrate (Figure, element 16) with components (Figure, elements 12) a casing comprising a 1st casing (Figure, element 22) and a 2nd casing (Figure, element 20), a 1st casing supporting the substrate (figure, element 30) and the 2nd casing having heatsink pedestals (figure, elements 26 left and right side) in thermal contact with components. It

would have been obvious to one of ordinary skill in the art at the time of the invention to place the substrates taught by Ohshima in the casing taught by Koors for the purpose of protecting the substrate while removing excessive heat from the components on the substrates.

With respect to claim 16 and with all the limitations of claim 15, Ohshima teaches that the organic substrate comprises multiple dielectric layers (Fig. 3, elements 32b-1-5) and the conductor is buried with in the dielectric layers of the organic substrate.

With respect to claim 17 and with all the limitations of claim 15, Ohshima teaches that the conductor patterns (Fig. 3, elements 32a-2-5) of the organic substrate is denser the conductor patterns (Fig. 3, elements 32a-1) of the ceramic substrate.

With respect to claim 18 and with all the limitations of claim 15, Ohshima teaches that the organic substrate comprises a second conductor (Fig. 3, element 34-1) and the common conductor overlays and is soldered (Fig. 3, element 38) to the second conductor.

With respect to claim 19 and 20 and with all the limitation of claim 15, Ohshima teaches all of the limitations including that the organic substrate comprises a through-hole (Fig. 3, element 36) and that it connects to the common conductor solderlessly. Ohshima does not teach that the through-hole is a plated through-hole. Plated through-holes are well known in the art and are used in many applications as connecting vias. It would have been obvious to one of ordinary skill in the art at the time of the invention to us plated through-holes for the purpose of making the electrical connection to the common conductor. For claim 20 Ohshima does not teach that the through-hole is

soldered to the common conductor. Soldering is well known in the art and is used in many circuit board applications to electrically bond and connect separate elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to solder the through-hole to the common conductor because then one could make the through-hole and common conductor as separate parts and solder them together during manufacture to electrically connect the two.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6703564 discloses a ceramic substrate with plate through holes, US Patent 6625037 discloses a ceramic substrate with vias and circuit component, US Patent 6784554 discloses an organic substrate with vais and circuit components.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IC

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